

The role of micro-shorts and electrode-film interface in the electrical transport of ultra-thin metallophthalocyanine capacitive devices

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The transport properties of metallophthalocyanine thin films are important ingredients in many technological applications. Ohmic conductance of thin film (15 nm to 90 nm) Co-phthalocyanine (CoPc) capacitive devices has been investigated in the temperature range of 40 K to 300 K. For Pd and V electrodes, the electrode-film (E-F) interface and metallic micro-shorts contribute substantially to the conductance with decrease in CoPc layer thickness. A quantitative model which describes E-F interface, CoPc roughness, micro-shorts, and the exponential temperature and thickness dependence of conductance was developed. Parameters obtained from this model are in good quantitative agreement with independent measurements. The model predicts a 15-20 nm lower limit for capacitive device thickness, below which the conduction is mainly controlled by shorts. In this regime, small changes in mean CoPc thickness result in drastic variation in device conductance. © 2012 American Institute of Physics. [<http://dx.doi.org/10.1063/1.4755762>]

Metallophthalocyanines (MPc) are molecular semiconductors possessing interesting structural,¹⁻⁴ optical,⁵⁻⁷ and electrical properties⁸ with many potential applications in solar cells,⁹⁻¹¹ organic light emission diodes (OLEDs),¹²⁻¹⁴ chemical sensors,¹⁵⁻¹⁸ and organic field effect transistors (OFETs).¹⁶⁻²⁰ Nonetheless, in spite of considerable progress in developing MPc devices, the mechanism underlying their electrical transport is understood poorly. MPc thin films show linear (ohmic) current-voltage (J-V) characteristic at low voltages and power law V dependence at high voltages. Following Gould,⁸ the power law behavior has been used to classify conduction as bulk- or electrode-limited, but the highly unusual behavior of MPc in the ohmic region was mostly overlooked.

Only recently, the ohmic region was explored in CoPc and CuPc thin film capacitive devices.²¹ To avoid impurities in the organic-layer (OL) and electrode-film (E-F) interfaces, which can cause order of magnitude changes in conductance, *in situ* ultra high vacuum fabrication (using organic molecular beam deposition-OMBD) was used. It was found that conductance decreases exponentially with OL thickness and increases exponentially with temperature. This exponential behavior was modeled in terms of thermally assisted sequential tunneling (TAST), which separates contributions to electrical transport from the E-F interfaces and the MPc OL. In particular, the device conductance is given as

$$G_{\text{TAST}}(T, L) = g_0 e^{-AL + (BL + C)T}, \quad (1)$$

where $G_{\text{TAST}}(T, L)$ is the average conductance per unit area, T is the temperature, L is the nominal OL thickness, and g_0 , A , B , and C are constants where g_0 is a proportionality constant dependant on both E-F interfaces and the OL, A , and B depend only on the properties of the OL, while C only on the properties of the E-F interfaces.²¹ However, this model does

not consider the effect of OL roughness or the possibility of micro-shorts in the film.

In this work, we studied the technologically important region of very thin CoPc films where OL roughness and E-F properties are essential. To do this, we measured conductance in capacitive devices with four different nominal OL thicknesses on two different electrode materials. The geometry of our devices consists of four V or Pd bottom electrodes (BEs), a CoPc OL, and a common top Pd electrode (TE) on c-cut sapphire substrate (see inset Fig. 2(a)). The bottom electrodes were all 40 nm thick, the CoPc OLs, were 15, 30, 50 or 90 nm thick, and the top electrode was 100 nm thick. Two metals with different work functions, Pd (5.6 eV) and V (4.3 eV), were chosen for BE to study different energy barriers for hole injection into the OL. Since CoPc behaves as a p-type semiconductor²² and has a highest occupied molecular orbital (HOMO) energy level of 5 eV,²³ the interface barrier is high (0.7 eV) for V/CoPc and low (-0.6 eV) for Pd/CoPc. Overall, the junctions measured were either Pd/CoPc/Pd or V/CoPc/Pd. For structural characterization, we measured Pd/CoPc and V/CoPc bilayers grown under the same conditions as the capacitive devices.

Since conductance can vary greatly due to impurities, special care was taken to ensure ultra clean E-F interfaces and high OL purity. The entire device was grown *in situ* in an OMBD system with a base pressure of 1×10^{-10} Torr using CoPc powder which was triple purified by gradient sublimation. TE and BE were deposited by electron beam physical vapor deposition while OL was deposited using a Knudsen effusion cell. The deposition rates for the BE and the OL were 0.3 Å/s and 0.1 Å/s, respectively. The Pd TE was deposited at a high rate (10 Å/s) to favor formation of larger, less mobile, metal clusters which diminished interdiffusion into the OL.²⁴ DC current-voltage measurements were performed in a two-probe configuration in darkness and vacuum of 1×10^{-4} Torr after a four-day stabilization period.

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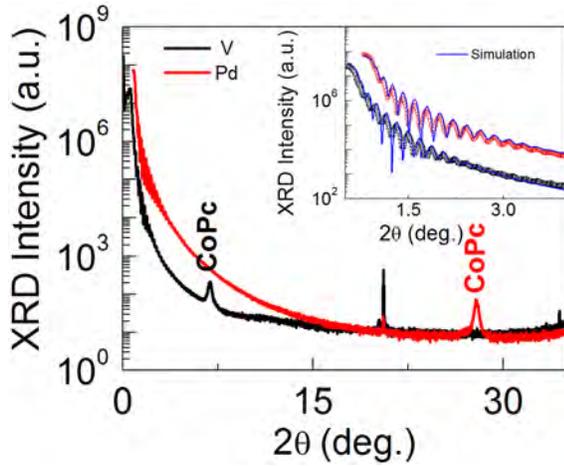


FIG. 1. XRD spectra of 50 nm CoPc films deposited on 40 nm V (black) and Pd (red) electrodes on c-cut Al_2O_3 substrate. The diffraction peak at 6.9° for the sample with the V (and the one at 27.9° with the Pd) electrode indicates that the CoPc growth at approximately 65° in a chevron structure (parallel) to the substrate plane. The inset shows the low angle oscillations and SUPREX fitting (blue line) from which Pd (1.1 nm) and V (1.4 nm) roughness values are obtained.

Structural characterization was made using x-ray diffraction (XRD, $\lambda_{\text{CuK}\alpha} = 1.54 \text{ \AA}$) and atomic force microscopy (AFM). XRD from V/CoPc and Pd/CoPc bilayers shows peaks at $2\theta = 27.9^\circ$ for Pd and $2\theta = 6.9^\circ$ for V (see Fig. 1), indicating that the CoPc molecules lie almost parallel to the electrode surface on Pd and in a chevron structure tilted 65° to the electrode surface on V. SUPREX software^{25,26} was used to fit the low angle x-ray oscillations in reflectivity which imply BE roughness of 1.1 nm for Pd and 1.4 nm for V (see inset in Fig. 1).

The temperature dependence of the conductance for various OL thicknesses for Pd and V BE is presented in Fig. 2. In the thickest devices (90 nm, Fig. 2(a)), both the Pd and V junctions have similar temperature dependence of the conductance indicating that the E-F interface contribution is insignificant and that electric transport is dominated by the OL. However, in the 50 nm device (Fig. 2(b)), two new effects emerge. First, the conductance of the Pd junction is higher than that of the V junction in the entire temperature range. Second, the temperature dependence deviates from the exponential behavior towards higher values for $T < 200 \text{ K}$. Qualitatively, the first effect is due to E-F interface becoming more important because the energy barrier difference between V/CoPc and Pd/CoPc starts to play a role. The second effect is due to a network of micro-shorts in the OL, which form a parallel conduction path. The micro-shorts contribute little to the overall conductance at high temperatures (when the OL is more conductive) but dominate at low temperatures (when the OL is more resistive). As expected, these effects are more pronounced in the 30 nm device, as shown in Fig. 2(c).

We developed a model that quantitatively describes the Mpc transport for all thicknesses measured in these experiments. This model accounts for micro-shorts, roughness, and TAST-predicted exponential behaviors. We assume that the OL has a distribution of thicknesses and that in a certain fraction of the junction area, there are metallic shorts (illustrated on Fig. 3). We then define the local conductance as

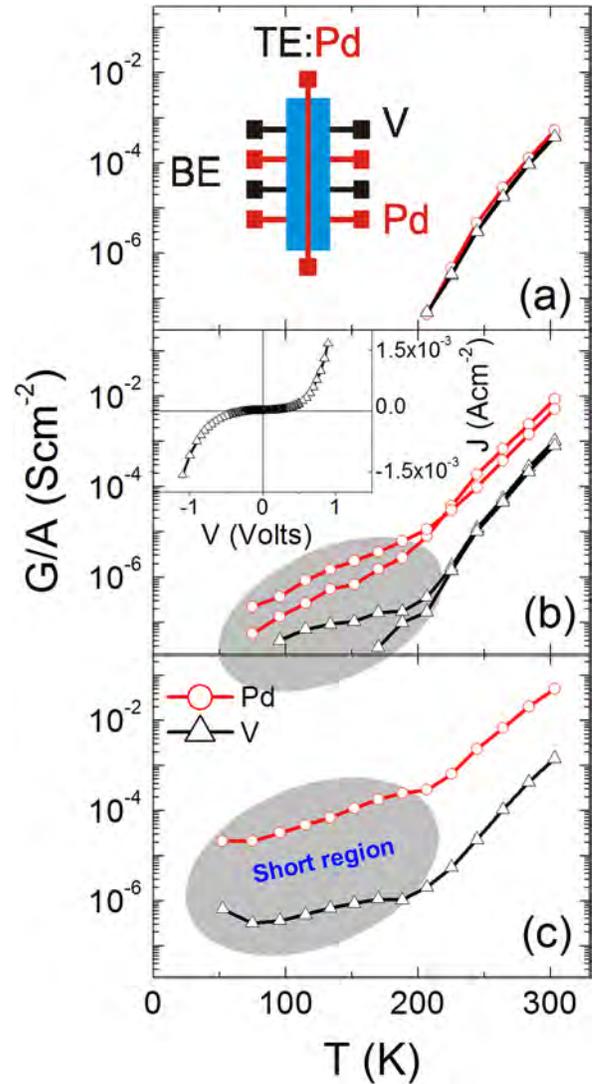


FIG. 2. Conductivity vs. temperature for Pd/CoPc/Pd (red circles) and V/CoPc/Pd (black triangles) junctions for 90 nm (a), 50 nm (b), and 30 nm (c) CoPc devices. Micro-shorts dominated regions are highlighted in gray. Inset (a) shows a schematic of the device consisting of two pairs of V and Pd BEs, a common CoPc film, and a Pd TE. Inset (b) shows an example of the J vs. V curves characteristics of the Pd and V BE junctions of the 50 nm CoPc device measured at 260 K. The $G/A = dJ/dV$ values were obtained from the linear regions of the J vs. V curves.

$$G_{\text{loc}}(T, y, L) = G_{\text{TAST}}(T, y)\Theta(y) + G_{\text{short}}(T, L)(1 - \Theta(y)), \quad (2)$$

where $G_{\text{loc}}(T, y, L)$ is the local conductance per unit area, $G_{\text{TAST}}(T, y)$ is obtained from Eq. (1) and $G_{\text{short}}(T, L)$ is the conductance per unit area of the micro-shorts perpendicular to the electrode. T is the temperature of the junction, y is the variable thickness of the OL (to be integrated over), a consequence of the roughness, and L is the mean thickness of the OL. $\Theta(y)$ is a step function whose value is 1 for positive y and 0 otherwise. Note that for a given y only G_{TAST} or G_{short} is non-zero. If y is positive, then the local transport is through the OL and is given by $G_{\text{TAST}}(T, y)$, but if y is non-positive, then the local transport is through a short and is given by $G_{\text{short}}(T, L)$. An actual junction will have a distribution of y values, positive ones describing the OL roughness while non-positive values describing the micro-shorts.

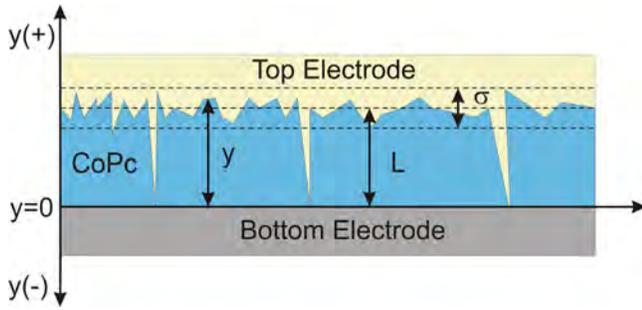


FIG. 3. Cross section schematics of a capacitive device showing the variables used in Eqs. (2)–(4). The variable y is negative when the local roughness is bigger than the mean thickness L . The standard deviation of the Gaussian thickness distribution, σ , is the roughness of the OL.

The average conductance per unit area for the entire junction is given by the convolution of the local conductance (Eq. (2)) with the thickness distribution function $f(y, \{\theta_i\})$,

$$G_{\text{rough}}(T, L) = \int_{-\infty}^{\infty} f(y; \{\theta_i\}) G_{\text{loc}}(T, y, L) dy, \quad (3)$$

where $\{\theta_i\}$ are the moments of the distribution function and $G_{\text{rough}}(T, L)$ is the observable conductance per unit area of the junction. The $(0, \infty)$ region of integration corresponds to the OL contribution to the conductance while the $(-\infty, 0]$ region of integration corresponds to the micro-shorts contribution to the conductance. For a Gaussian thickness distribution, $G_{\text{rough}}(T, L)$ can be integrated into the following form:

$$G_{\text{rough}}(T, L) = \frac{1}{2} \left[g_0 e^{-AL + (BL+C)T + \frac{1}{2}(A-BT)^2 \sigma^2} \times \left(1 + \text{erf} \left[\frac{(BT - A + L/\sigma^2) - \frac{\sigma}{\sqrt{2}}}{\frac{\sigma}{\sqrt{2}}} \right] \right) + G_{\text{short}}(T, L) \text{erfc} \left(\frac{L}{\sqrt{2}\sigma} \right) \right], \quad (4)$$

where σ is the standard deviation of the thickness distribution (OL roughness), erf is the error function, and erfc is the complementary error function.

Fig. 4 presents a comparison of this model with the experimental data. $G_{\text{short}}(T, L)$ (perpendicular to the electrode) was estimated from experimental four-probe measurements of in-plane conductivity of Pd and V BE. Junctions with V BE were fitted with V electrode G_{short} while junction with Pd BE were fitted with Pd electrode G_{short} . Values for roughness were fitted independently for each thickness/BE material. The fit itself was made using MATLAB implementation of Nelder-Mead simplex algorithm (`fminsearch`). Both the OL

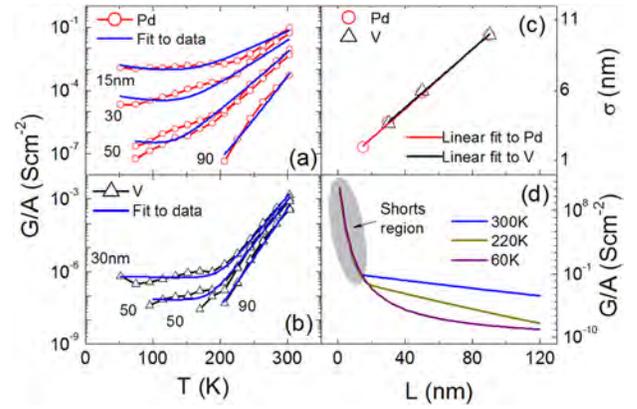


FIG. 4. (a) and (b) show the measured conductivity G/A vs. temperature dependence for Pd (red circles) and V (black triangles) together with their fits (blue line). The numbers next to each curve indicate CoPc film thickness in nm. (c) shows roughness (σ) dependence on thickness as fitted by the model for Pd (red circles) and V (black triangles) BEs. The red and black lines are linear fits of the data. (d) Shows the model prediction for conductivity as a function of CoPc layer thickness at 300, 220, and 60 K for a Pd junction. In all cases, shorts dominate transport below $L \sim 17$ nm.

and the shorts dominated portion of the G - T dependence are well fitted by our model. The deviation of conductance from the exponential behavior below $T < 200$ K is determined by the temperature dependence of the metal shorts (G_{short}) while at high temperature conductance is determined by parameters g_0 , A , B , and C from TAST. Fits to Pd BE conductance data are presented in Fig. 4(a) while fits to V BE data are shown in Fig. 4(b). Parameters obtained from the fits are presented in Table I.

Table I shows that B and C obtained from these fits are consistent with those previously reported²¹ for Pd/CoPc/Pd and Au/CoPc/Au, indicating that the temperature dependence of conductivity above 200 K is largely independent of roughness. The fitted roughness for both BE are remarkably similar and increase linearly with thickness (see Fig. 4(c)) with the coefficients 0.106 nm/monolayer for Pd and 0.104 nm/monolayer for V. These results agree with previous studies for CoPc on Si substrate (0.05 nm/monolayer)¹⁷ and our recent independent AFM measurements.

Using the linear dependence of roughness on OL thickness, Fig. 4(d) shows the predicted thickness dependence of conductance at various fixed temperatures for Pd BE. We found two thickness regimes, each characterized by its own exponential dependence of conductance on thickness. The first region ($L > 17$ nm for $T = 300$ K) is not heavily impacted by micro-shorts and can be understood in terms of simple exponential behaviors from TAST. However, the second region ($L < 17$ nm for $T = 300$ K) is micro-shorts dominated and has the highest sensitivity to the thickness of the OL. This high sensitivity to OL thickness presents an important challenge in creating reproducible ultra-thin MPC

TABLE I. Fitted parameters for V and Pd BE in thin capacitive CoPc devices.

BE material	g_0 (S cm ⁻²)	A (nm ⁻¹)	B (nm ⁻¹ K ⁻¹)	C (K ⁻¹)	$\sigma_{L=15}$ (nm)	$\sigma_{L=30}$ (nm)	$\sigma_{L=50}$ (nm)	$\sigma_{L=90}$ (nm)
V	3.45×10^{-12}	0.11	0.00030	0.068	... ^a	3.66	5.96	9.93
Pd	3.5×10^{-4}	0.34	0.00091	0.021	1.94	3.72	5.85	9.93

^aJunction defective.

capacitive devices as it places very stringent constraints on device uniformity and thickness accuracy.

In summary, contributions of roughness, micro-shorts, and TAST to overall electrical transport in sub 100 nm CoPc capacitive devices were studied. With decreasing OL thickness, the energy barrier at the E-F interface and metallic micro-shorts through the OL become important. The model presented here describes quantitatively the experimental results and predicts that roughness increases linearly with thickness in agreement with independent transport and AFM measurements. Finally, the model establishes a lower thickness limit of 15-20 nm for the design of capacitive organic devices, below which shorts start influencing the conduction mechanism and should be taken into account.

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